

Application No.: 09/577,932  
Amendment Under 37 C.F.R. §1.111 dated December 20, 2004  
Response to the Office Action of October 18, 2004

### REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1 – 5 and 13 – 18 are pending in this application, new claims 16-18 having been added by the present Amendment. Claims 1 – 5, 14 and 15 stand rejected. Claim 13 has been allowed. Claim 3 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form. No new matter has been added. The rejections set forth in the Office Action are respectfully traversed below.

New claims 16 – 18 correspond to claims 1, 14 and 15, respectively, rewritten to include the features of claim 3. Each of claims 16 - 18 should be in condition for allowance in view of the October 12, 2004 telephonic interview during which the Examiner indicated that claims 1, 14 and 15 would be in condition for allowance if amended to include the features of claim 3.

### Claim Rejections – 35 U.S.C. §102

Claims 1 – 5, 14 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over **Beddingfield** (USP 5,726,502) in view of **Matsuda et al.** (USP 5,757,078). For the reasons set forth in detail below, this rejection, to the extent it is considered to apply to the present claims, is respectfully traversed.

Initially, it is noted that in the “Response to Arguments,” the Examiner asserts that the language “being configured to be provided with external connection electrodes” (claims 1 and 14) is functional language, and has not given this language any patentable weight.

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Claims 1 and 14 have been amended hereby to positively recite the external connection electrodes as a *structural* feature of the claimed invention. It is respectfully submitted that, in view of the amendments to claims 1 and 14, the external connection electrodes should be given patentable weight.

#### The Beddingfield reference

The Examiner responds to the remarks set forth in the August 5, 2004 Amendment by asserting that Fig. 7 of **Beddingfield** "clearly shows . . . the plurality of metal posts (108) and the plurality of electrode pads (104) have a flat top surface."

Although the description of **Beddingfield** is somewhat ambiguous, it appears that the Examiner is correct in asserting that Fig. 7 of **Beddingfield** illustrates the I/O bump 108 ("metal post") as having a flat top surface. Specifically, Fig. 7 of **Beddingfield** illustrates a process step in forming the bumped semiconductor device. **Beddingfield** describes that after the device shown in Fig. 7 is formed, the bump metallurgy is reflowed (see Fig. 6, step 90), wherein the bumps take on a new spherical shape, as illustrated in Fig. 8 (see column 7, lines 23 – 24). Further, column 6, lines 16 – 19 of **Beddingfield** state "Fig. 7 is used for clarity in comparing the bump formation process to the *final bump shape* shown in Fig 8."

However, on the other hand, the **Beddingfield** reference indicates that the bumps 108, 110 shown in Fig. 7 are *not* reflowed *unless* the metallurgy used to form the bumps is C4 or plated bulk metallurgy (see column, lines 19 – 23 and 45 – 46). Moreover, column 9, lines 8 – 11 of **Beddingfield** state "the alignment bumps should substantially maintain their *originally*

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*formed shape* or reflow shape and not experience the extent of physical damage that I/O bumps experience.”

Therefore, it appears that the embodiment shown in Fig. 7 can be the final shape of the I/O bump 108, and that Examiner’s interpretation of the I/O bumps 108 having a flat top surface is reasonable.

#### **Claims 1 and 14**

Initially, we note that claims 1 and 14 differ in that claim 1 recites, in addition to each element of claim 14, “wherein the mark member is made of the same material as the metal posts.” Therefore, claims 1 and 14 will be discussed together.

Claims 1 and 14 recite “external connection electrodes contacting the respective metal posts.” Support for this recitation is provided, e.g., as shown in Fig. 2 of the present application, as solder balls 22 formed on the metal posts 16.

The Examiner considers the I/O bumps 108 of **Beddingfield** to correspond to the claimed metal posts. However, the I/O bumps 108 shown in Figs. 7 and 8 are not in contact with external connection electrodes. In fact, the I/O bumps 108, which may be solder balls, serve as external connection electrodes.

The Examiner asserts that the conductive I/O pad 41 on mounting substrate 34 (shown in Fig. 2 of **Beddingfield**) corresponds to the claimed external connection electrodes (see Office Action, page 2, final line). However, in contrast to the present invention, the conductive I/O pad

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41 does not contact the I/O bump 36 shown in Fig. 2 of **Beddingfield**. Instead, there is eutectic solder 42 between the I/O bump and the I/O pad 41.

Thus, it is respectfully submitted that neither **Beddingfield** nor **Matsuda et al.** disclose or suggest a semiconductor device having a structure wherein external connection electrodes contact respective metal posts.

Further, it is respectfully submitted that there is no motivation or incentive to combine **Matsuda et al.** with **Beddingfield**. In rejecting claims under §103, the Examiner must provide a reason why one having ordinary skill in the relevant art would have been led to combine the prior art references to arrive at the claimed invention. Such reason supporting the combination must stem from some teaching, suggestion, or incentive in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. However, where no reasonable teaching, suggestion or incentive exists for the proposed combination, a *prima facie* case of obviousness will not have been established.

The Examiner acknowledges that **Beddingfield** does not disclose a redistribution layer and applies **Matsuda et al.** for the teaching of a redistribution layer. However, **Matsuda et al.** is directed to a semiconductor device including multiple solder bumps having a semi-spherical shape (see, e.g., Figs. 4 and 5), which bump structure is quite different from the I/O bump 108 structure shown in Fig. 7 of **Beddingfield** having a flat surface. Further, **Beddingfield** is related to an alignment bump structure, while **Matsuda et al.** is completely unrelated to a semiconductor device having alignment marks.

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Therefore, the **Beddingfield** and **Matsuda et al.** references are directed to different functional aspects of I/O bumps having different bump structures. In view of the structural and functional differences between **Beddingfield** and **Matsuda et al.**, it is submitted that there is no motivation for combining the **Beddingfield** and **Matsuda et al.** references, and that the combination is the result of hindsight using applicants own teachings.

#### Claims 15

Claim 15 has been amended to improve form and clarify relationships between elements.

Independent claim 15 recites features similar to claims 1 and 14, and further recites that the metal posts form both electrodes and alignment marks. More particularly, in accordance with the embodiment recited in claim 15, when a protruding electrode is attached to a top of the metal post, the protruding electrode and the metal post form an electrode part. The metal post lacking the protruding electrode attached to the top of the metal post forms an alignment mark.

The Examiner considers the I/O bump 108 of **Beddingfield** to correspond to the claimed metal posts and the alignment bump 110 to correspond to the claimed mark member (see Office Action, page 6).

However, the **Beddingfield** device has a structure that is different from that of the invention recited in claim 15. More particularly, in accordance with the invention recited in claim 15, the metal posts, which form the mark member and the electrode part, are formed on the electrode pads of the redistribution layer. For example, as disclosed on page 34, lines 4-9 of the

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present application, the mark member is electrically connected to one of the electrode pads of the semiconductor device.

However, in contrast to an embodiment of the claimed invention, the alignment bump 110 disclosed by **Beddingfield** is not formed on an electrode pad, and instead, is formed on polyimide or a passivation layer 103 because the alignment bump 110 of **Beddingfield** is *not electrically coupled to the semiconductor die or the integrated circuitry formed thereon* (see column 6, lines 49-53).

Moreover, it is submitted that **Beddingfield** does not disclose or suggest the claimed electrode part formed of the metal post and protruding electrode attached to a top of the metal post. The I/O bumps 108 of **Beddingfield**, which are considered by the Examiner to correspond to the claimed metal posts, do not include a protruding electrode attached to a top of the I/O bumps 108.

Furthermore, **Matsuda et al.** do not alleviate any of the above-noted deficiencies of **Beddingfield**.

#### Claim 4

Claim 4 has been amended to clarify the relationship between the claimed electrode pads and the redistribution layer. Specifically, claim 4 has been amended to recite that the electrode pads are formed at predetermined positions on the redistribution layer, and that the mark member is formed on the redistribution layer. Support for these changes is found, e.g., on page 24, lines 21-22 and lines 34-36 of the present application.

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With respect to the rejection of claim 4, the Examiner asserts that I/O bumps 108 correspond to the claimed electrode pads and the alignment bumps 110 correspond to the claimed mark member (see Office Action, page 4).

In contrast to an embodiment of the presently claimed invention, both the I/O bump 108 and alignment bump 110 of **Beddingfield** are formed on pad limiting metallurgy 104. **Beddingfield** does not teach or suggest that the I/O bump and alignment bump 110 are formed on a redistribution layer. For example, in accordance with embodiments of the present invention, forming the mark member on a redistribution layer advantageously allows the mark member to be connected to a terminal in the redistribution layer (see page 34, lines 9-15).

Further, **Matsuda et al.** do not alleviate any of the above-noted deficiencies of **Beddingfield**.

For all the reasons set forth above, it is respectfully submitted that neither **Beddingfield** nor **Matsuda et al.**, whether taken alone or in combination, disclose, suggest or render obvious the presently claimed invention. Reconsideration and withdrawal of the rejection under §103 are respectfully requested.

#### CONCLUSION

For the reasons set forth in detail above, it is respectfully submitted that all pending claims are in condition for allowance. An indication of allowability of all pending claims is respectfully requested.

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If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

In the event that any fees are due in connection with the filing of this paper, please charge any fees to Deposit Account No. 50-2866.

Respectfully Submitted,

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